I'm sorry I rooted your Smart House, I wish it was mine

A modular anthology guide to go from zero to hardware hacking hero (or at least learn how to pop open a shell on your Smart Fridge)

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Part 1

Theory

Agenda

Part 2



Practice



Agenda Part 1: Essential Info for Hardware Hacking

Part 1:

- 1. An introduction, including definitions of important terms
- 2. Methodology and motivations for reverse engineering embedded devices
- 3. An overview of electrical engineering fundamentals necessary to understand serial communication on an embedded device.
- 4. An overview of serial communication protocols

Agenda Part 2: The Starving Artist's Guide to Building a Hardware Hacking Lab

Part 2: Creating your hardware hacking lab and reverse engineering toolkit



Agenda Part 3: Let's break some stuff!

- Part 3: Proof of Concept: Foscam surveillance camera
- An overview of hardware hacking techniques
 - a. Definitions and illustrations of hardware
 - b. Identifying test points
 - c. Soldering
 - d. Dumping contents of serial flash chips
 - e. Patching contents of serial flash chips
- Conclusion \bullet
- References

Motivations

Why learn about hardware hacking and embedded device security?

• Having the security of your organization compromised because no one patched the firmware on the Smart Fridge in the break room is not a cute look!!

"Patching your firmware — is always in style."





Notivations Why learn about hardware hacking and embedded device security?

- look!!
- Learn how to create Mr. Robot-esque art installations using an IoT art botnet

 Having the security of your organization compromised because no one patched the firmware on the Smart Fridge in the break room is not a cute



Reverse Engineering Methodology General Overview

- Reconnaissance / research reading data sheets for the device, as well as data sheets for specific hardware components on the device PCB
 - 1. Compile relevant related research on the device, including current CVEs, research papers or talks
- 2. Identification of access points for the device, including JTAG, SPI, and UART
- 3. Serial console setup and analysis
- 4. Obtain firmware image
- 5. Static and dynamic analysis of firmware image
- 6. Identification of vulnerabilities on the device
- 7. Exploit development

Reverse Engineering Methodology (but make it Euclidean)

Initial Reconnaissance / Research on device Identifying areas of interest on PCB for UART, SPI, JTAG, etc

Exploit Development

Identify Vulnerabilities

Serial Console Setup and Initial Analysis

> Obtain firmware image

Firmware Analysis



Presentation Format

Circuit Schematic Symbols: A Rosetta Stone



Circuit Schematic Continued: Logic Gates





Embedded devices

Embedded device

A computer, in miniature





Firmware version: 1.11.1.16





A handy sticker with our default admin credentials



FOSCAM Model: FI9821W V2 MAC ID: C4D65539337D DDNS:fc9132. myfoscam.org User name(default):admin Password(default):(blank) FCC ID: ZDEFI9821W S/N:821AW1406026032





Opening up the device





PCB of Foscam



Unique features/challenges of hacking embedded devices

- 1. It's headless need to set up a serial console to see terminal during important processes
- 2. It runs an architecture that will not be x86. I learned ARM assembly and have been working primarily with devices that run on that architecture throughout my work on this project. There is also MIPS, PowerPC, others



Firmware



Similar to an OS kernel

Firmware

Intermediary piece of software that serves as the interface between software/ hardware



obtaining the firmware: directly from vendor website

• •	Foscam S	Support - Downloads	× +			
←	\rightarrow C \triangleq fost	cam.com/download	ds/firmware_details	.html?id=43	\$ \$	🔒 Incog
★ B	Bookmarks 📄 New	/s 📄 Popular 📄 2014/04/08	Imported From Sa וב.סועום	comp_geometry C Programming La Miscellaneous g that visitor and operator can brower to Settings interface if not install the plug in.	ersion	.
	V-2.11.1.6	2014/02/19	16.6MB	1) Support turnning on/off the IR LEDs in schedul ed time; 2) Enhance the security when using CGI to do snapshot; 3) Enhance the ONVIF feature; PI ease refer to more new features and improveme nts in the "Read me" text document in the firmw are package.	Only application firmware version 1.11.1.18 can be upgraded to this version;	Ŧ
	V-1.11.1.18	2013/11/13	16.0MB	1) Support ONVIF; 2) Support uploading snapsho ts to FTP server in fixed time interval; 3) Enhace t he SD card management feature; Please refer to more new features and improvements in the "Re ad me" text document in the firmware package.	Only application firmware version 1.11.1.16 can be upgraded to this version.	Ŧ
	V-1.11.1.16	2013/08/22	7.70MB	1) Add the new SD management feature under W indows OS; 2) Improve the image quality for snap shot; 3) Improve the image quality of the MJPEG stream;Please refer to more new features and im provements in the "Read me" text document in t he firmware package.	Only for FI9821W V2	Ł



:~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/firmware_binaries# file FI9821A_app_ver1.11.1.16 .bin FI9821A_app_ver1.11.1.16.bin: openssl enc'd data with salted password

file FI9821A_app_ver1.11.1.16.bin

output from file command indicates that the firmware image is encrypted with opensal



ord binwal	HEXADECIMAL %0×0 furefile	DESCRIPTION OpenSSL encryption, sal	ť
Scan Time:curi Target File: 821A_app_ver1 MD5 Checksum: Signatures:	2021-05-10 01:: /root/Desktop/0 .11.1.16.bin 23c03a5d0d2a1d 391	18:22 dc207_hardware_talk_demo 7e66b373a82159d6ec	
<pre>root@kali:~/D FI9821A_app_v</pre>	e <mark>sktop/dc207_har</mark> e er1.11.1.16.bin	dware_talk_demo/_FI9821W	_'

binwalk -v FI9821A_app_ver1.11.1.16.bin

binwalk also tells us that the file is encrypted with openssl

V2-1.11.1.16-20130822.zip.extracted/firmware_binaries# binwalk -v

_FI9821W_V2-1.11.1.16-20130822.zip.extracted/firmware_binaries/FI9

ed, salt: 0×26C939CA4C17754E



Firmware decryption script for Foscam firmware images

mcw0 Github

• • • • 🖓 PoC/de	crypt-foscam.py at mas × +	
$\leftarrow \rightarrow C$ \bullet gi	thub.com/mcw0/PoC/blob/master/decrypt-foscam.py	Q 🕁 👼 Incog
🛨 Bookmarks 🗎 Ne	ws 🛅 Popular 🛅 Imported From Sa 🛅 comp_geometry 🛅 C Programming La 🛅 Miscellaneous	
🖵 mcw0 / PoC		Ĵ Notifications ☆ Star 355 양 Fork
<> Code ্ণ Pull	requests 🕟 Actions III Projects 🕕 Security 🗠 Insights	
	° master - PoC / decrypt-foscam.py / <> Jump to -	Go to file
	marcelrv fix typo	Latest commit c9d6aab 6 days ago 🛛 History
	ম 2 contributors 💮 🊱	
	205 lines (183 sloc) 4.74 KB	Raw Blame 🖵 🖉 🖞
	<pre>1 #!/usr/bin/env python2.7 2 # 3 # Small OpenSSL wrapper to looping different encryption keys/digest and cipher on Foscam IPC Firmware images. 4 # 5 # //bashis 2018 6 # 7 import os 8 import subprocess 9 import sys 10 import argparse 11 12 CMD = "openssl enc -d CIPHER -in IN_FILE -out OUT_FILE -md DIGEST -k 'OPENSSL_KEY'" 13 14 ifname == "main": 15 16 INF0 = '[bashis 2018 <mcw eu="" noemail="">]' 17 18 try: 19 arg_parser = argparse.ArgumentParser(20 promesys argu[0]</mcw></pre>	



Firmware decryption script for Foscam firmware images

list of potential decryption keys

mcw0 Github

```
ENC_KEYS = {
                               # Decrypt: HI3518A_ddr256M_sys_ver 1.4.1.7 / 1.4.1.8 + FI9x Ver 1, recovertool
       0:'Wxift*',
       1:'Wxift*v2', # FW Decrypt 'B' AKA 'FosBaby'
       2:'WWxift*',
       3:'WWxift*v2', # FW Decrypt 'B' AKA 'FosBaby'
       4:'Wyift*',
       5:'Wyift*v2', # FW Decrypt 'C' AKA FI9903P
       6:'WWyift*',
       7:'WWyift*v2', # FW Decrypt 'C' AKA FI9903P
       8:'Wzift*',
       9:'Wzift*v2',
       10:'WWzift*',
       11:'WWzift*v2', # FW Decrypt 'E' AKA 'C1'
       12:'Weift*',
       13:'Weift*v2',
       14:'WWeift*',
       15:'WWeift*v2', # FW Decrypt 'G' AKA 'C1-Lite'
       16:'Pxift*', # exist (config)
       17:'Pxift*v2',
       18:'PPxift*',
       19:'PPxift*v2',
       20:'Xti1f*', # recovertool
       21:'Xti1f*v2',
       22:'XXti1f*',
       23:'XXti1f*v2',
       24:'Ktf1g*', # exist (config)
       25:'Ktf1g*v2',
       26:'KKtf1g*',
       27:'KKtf1g*v2',
```



decrypted firmware image contents

kali:~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/decrypted_firmware_dir# ls app.tar boot.sh FWUpgradeConfig.xml sfwupgrade.md5seresolv.conf app :~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/decrypted_firmware_dir# cat resolv.conf nameserver 192.168.1.1 nameserver kali:~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/decrypted_firmware_dir#

root@kali:~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/decrypted_firmware_dir/app/bin# strings FirmwareUpgrade/ [grep =n)==colort=in"openssl" penssl enc -d -aes-128-cbc -k Wxift* -in %s > %s 184:0 exist abnormally 185: decryption fail, result=%d 186:FWUpgrade

strings in the FirmwareUpgrade binary reveal that the decryption command is hardcoded, along with key



FirmwareConfig.xml

Tells us that we only have one partition of the device, have to extract firmware to directly from chip to explore further

```
:~/Desktop/dc207_hardware_talk_demo/_FI9821W_V2-1.11.1.16-20130822.zip.extracted/decrypted_firmware_dir# cat FWUpgradeConfig.xml
<?xml version="1.0" encoding="UTF-8" standalone="yes" ?>
<!DOCTYPE boost_serialization>
<boost_serialization signature="serialization::archive" version="9">
<mConfig class_id="0" tracking_level="0" version="0">
        <romPart class_id="1" tracking_level="0" version="0">
               <isExist>0</isExist>
               <fileName></fileName>
               <mainVer>1</mainVer>
               <subVer>0</subVer>
               <revision>0</revision>
       </romPart>
        <nsbootPart>
               <isExist>0</isExist>
               <fileName></fileName>
               <mainVer>1</mainVer>
               <subVer>0</subVer>
               <revision>0</revision>
       </nsbootPart>
       <ubootPart>
               <isExist>0</isExist>
               <fileName></fileName>
               <mainVer>1</mainVer>
               <subVer>0</subVer>
               <revision>0</revision>
       </ubootPart>
       linuxPart>
               <isExist>0</isExist>
               <fileName></fileName>
               <mainVer>1</mainVer>
               <subVer>0</subVer>
               <revision>0</revision>
       </linuxPart>
        <appPart>
               <isExist>1</isExist>
```



boot.sh

#init network
#if [-e /mnt/mtd/debug]; Then proc_men_t infosec learn web_securi
#ifconfig eth0 down
#ifconfig eth0 hw ether 004657166815
#ifconfig eth0 up
#ifconfig eth0 192.168.1.15
#mount -t nfs -o nolock 192.168.1.223:/home/foscam/nfs /mnt/nfs
#fi
ifconfig lo up
#telnetd
rm _rf /mnt/mtd/app/bip/lighttpd=1 / 30-bi

cd /tmp/ cp /mnt/mtd/app/www.tar.gz . tar -zxf /tmp/www.tar.gz -C /tmp/www rm -f /tmp/www.tar.gz cp /mnt/mtd/app/bin/cgi-bin/* /tmp/www/cgi-bin/ ln -s /mnt/mtd/app/plugins/FSIPCam.cab /tmp/www/FSIPCam.cab ln -s /mnt/mtd/app/plugins/plugins.crx /tmp/www/plugins.crx ln -s /mnt/mtd/app/plugins/plugins.pkg /tmp/www/plugins.pkg ln -s /mnt/mtd/app/plugins/plugins.xpi /tmp/www/plugins.xpi #cp /mnt/mtd/app/bin/* /bin/ #cp -rf /mnt/mtd/app/bin/ppp /bin/

#echo 8192 > /proc/sys/vm/min_free_kbytes
cp /mnt/mtd/app/bin/ftpd/FtpPortConfig.xml /mnt/mtd/app/config/
mkdir /usr/local/pureftpd
mkdir /usr/local/pureftpd/etc
cp /mnt/mtd/app/bin/ftpd/pureftpd.passwd /usr/local/pureftpd/etc/
cp /mnt/mtd/app/bin/ftpd/pureftpd.pdb /usr/local/pureftpd/etc/

#telnetd
rm -rf /mnt/mtd/app/bin/lighttpd-1.4.30-hi
mkdir /usr/local

cp -R /mnt/mtd/app/bin/lighttpd-1.4.31-hi /usr/local/



BY OFFENSIVE SECURITY



boot.sh continued

```
cd /mnt/mtd/app/modules
./load3518 Hi
 eval $(cat /mnt/mtd/app/config/PTZConfig.xml) grep 'SelfTestMode' awk -F ">" '{print $2}' awk -F "<" '{printf("ptzstate_xmlcfg=%d",$1
    eval $(cat /mnt/mtd/app/config/PTZConfig.xml | grep 'PreHorPos_Appointed' | awk -F ">" '{print $2}' | awk -F "<" '{printf("prehorpos
        eval $(cat /mnt/mtd/app/config/PTZConfig.xml | grep 'PreVerPos_Appointed' | awk -F ">" '{print $2}' | awk -F "<" '{printf("prever
            /sbin/insmod /mnt/mtd/app/modules/extdrv/fos_ptz.ko ptz_state=$ptzstate_xmlcfg horizen_desire_pos=$prehorpos_xmlcfg vertical_d
esire_pos=$preverpos_xmlcfg
if [ $? -ne 0 ]
  echo "insmod fos_ptz.ko fail, now try default param"
  /sbin/insmod /mnt/mtd/app/modules/extdrv/fos_ptz.ko ptz_state=1
/sbin/insmod /mnt/mtd/app/modules/hirtc.ko
/sbin/insmod /mnt/mtd/app/modules/wdt.ko default_margin=5
hwclock -s
mkdir -p /etc/Wireless/RT2870STA
cp -f /mnt/mtd/app/etc/RT2870STA.dat /etc/Wireless/RT2870STA/
mkdir /tmp/www
#cp -rf /mnt/mtd/app/lib/* /lib/
mkdir /etc/ppp
mkdir /mnt/windows
                                                                                                                        21,1
```



decompressed app.tar archive





contents of /bin/ dir

rootijkali:~	/Desktop/dc207_ha	rdware_talk_demo/_FI	9821W_V2-1.	11.1.16-2013082	2.zip.extracted/	/decrypted_firmware_dir/app/bin# l	S
cgi-bin 📊 c	FirmwareUpgrade	iwlist	MsgServer	ррр	rtctool	watchdog	
codec	flashcp	iwpriv	msmtp	pure-ftpd	RtspServer	webService	
ddnsclient	ftpd hy	lighttpd	ntpclient	pure-pw	storage	wpa_cli	
devMng	iwconfig	lighttpd-1.4.31-hi	openssl	releaseShm.sh	UDTMediaServer	wpa_supplicant	


Reverse Engineering Methodology (but make it Euclidean)

Initial Reconnaissance / Research on device Identifying areas of interest on PCB for UART, SPI, JTAG, etc

Exploit Development

Identify Vulnerabilities

Serial Console Setup and Initial Analysis

> Obtain firmware image

Firmware Analysis







Integrated Circuits

Processor Candidate

Find data sheet for specified chip, identify architecture etc.



Processor candidates, opposite side of PCB

Identified Processor chip: H1358





Flash chip candidates

Find associated data sheets for part number, cross reference with other device specs



Flash chip candidates, opposite side of PCB

Identified Flash Chip: MX25L12835F





Datasheets

MP1484 Voltage Regulator



The Future of Analog IC Technology

The MP1484 is a monolithic synchronous buck regulator. The device integrates top and bottom $85m\Omega$ MOSFETS that provide 3A of continuous load current over a wide operating input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on and in shutdown mode, the supply current drops below $1\mu A$.

The MP1484 is PIN compatible to the MP1482 2A/18V/Synchronous Step-Down Converter.

MP1484 3A, 18V, 340KHz Synchronous Rectified Step-Down Converter

FEATURES

- 3A Continuous Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated 85mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 20V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOIC Package

APPLICATIONS

- FPGA, ASIC, DSP Power Supplies
- LCD TV
- Green Electronics/Appliances
- Notebook Computers

"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.



Datasheets

MX25L12835F



MX25L12835F

MX25L12835F

3V, 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO[®] (SERIAL MULTI I/O) FLASH MEMORY



Datasheets

MX25L12835F Serial Flash



MX25L12835F

3. PIN CONFIGURATIONS



16-PIN SOP (300mil)



8-WSON (6x5mm, 8x6mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION			
CS#	Chip Select			
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)			
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)			
SCLK	Clock Input			
WP#/SIO2	Write protection Active low or Seria Data Input & Output (for 4xI/O read mode)			
RESET#/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)			
VCC	+ 3V Power Supply			
GND	Ground			
NC	No Connection			
DNU	Do not use			

Notes:

- 1. RESET# pin has internal pull up.
- When using 1I/O or 2I/O (QE bit not enable), the DNU/SIO3 pin of 16SOP can not connect to GND. Recommend to connect this pin to VCC or floating.



Simplified View of Communication between two computers



UART headers

Typically 4 pins in a row



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UART



Universal Asynchronous Receiver/Transmitter

3 pins: TX RX GND





TTL (Transistor-Transistor Logic)

-> TTL or Transistor - Transistor Logie is a standard for defining logic states based on threshold roltage levels ATTL relies on circuits built from bipofar transistors to achieve switching and maintain logic states The majority of systems in everyday life use 3.3V or 5V TH levens -> VOH is the minimum output high voltage -> the output voltage of the device driving MITGH will always be at least 2.7V -Vон 2.7V_ 2.0V-V-TH -- > VIH is the minimum input high voltage -> basecally any vollage that is at least 2V - VIL 0.8V -0.4 V- VoL will be read in as a OV ____ GND logie 1 (HIGH) to a Standard 5V TTL TTL device ~ Vor is the maximum ->VIL is the output low voltage Montimen impret Lau voltage → a device to send a logic lelow 0.4 V trying to will be $\rightarrow \alpha$ - any input signal that is below 0.87 will le le considered a logic (LOW) when read into a derrice

Serial Console

Serial Console

The serial console uses a serial port connection to access a computer, allowing a user to interact with a device and issue commands through a terminal emulator



Serial Console

Serial terminal programs include (but are not limited to): minicom, cutecom, screen, Putty, etc.

setup command for minicom: sudo minicom -s (pictured to the right)

Enter configuration settings for the following: baud rate, frame size, parity, start/stop bits

8N1 is a fairly common configuration for frame size, parity, and start/stop bits

		ing_recourses	
A - Serial Device B - Lockfile Location C - Callin Program D - Callout Program	: /dev/ttyUSB0 : /var/lock :		
E - Bps/Par/Bits F - Hardware Flow Control G - Software Flow Control H - RS485 Enable I - RS485 Rts On Send J - RS485 Rts After Send K - RS485 Rts After Send K - RS485 Rx During Tx L - RS485 Terminate Bus M - RS485 Delay Rts Before N - RS485 Delay Rts After Change which setting?	I 115200 8N1 No No No No No No No No No No No data	e GN kringlecon_3 e intervention t_rb output wav_ test	plaid_c dc207_ are_tal





SPI



Serial Peripheral Interface

4 pins: CS (Chip Select) CLK (Clock) MISO/DO (Master In/Slave Out, Data Output) MOSI/DI (Master Out/Slave In, Data Input)

that Line ("Slave Select") is the **S** to a specific slave device communicates he read to wake up it and cause to send / reteive dater; it is used when multiple Slave are present devices Slave device Master device SCK SCK MOSI MOSI MISO W120 55 SS SCK Mosi 10 Q 0 Ox 53 = ASCTI (ISO 00 Ò 10 Ox46 = ASCII 55 after Lost byte stat or received -) the SS line is normally from the SPI bus (meaning held high which discoments it lion





Lab Materials



Essentials

Jumper Wires

M/M, M/F, F/F Variety for myriad uses





Header pins

Pitch on pins that you use should match the pitch of pins on the board





Serial-to-USB Converter

Serial-to-TTL adapter with 3.3V and 5V settings



Multimeter

For testing continuity between points, verifying pins





Soldering Iron

Temperature-controlled, to adjust for different types of solder



Soldering Iron Stand

For supporting the soldering iron



Flux

Heraclitus <3



ROSIN PASTE FLUX

WARNING: Harmful if swallowed; Irritating to eyes, respiratory system, and skin. Please see back for more info.

Contact Us: 508-668-6044





Solder

Leaded or lead-free

Soldering wick

a copper vacuum for excess solder

Miscellaneous items for soldering workbench

- Kitchen sponge or brass sponge
- Razor or straight edge
- Isopropyl alcohol
- A workbench
- Silicon baking sheets
- A vice grip or a Helping Hands



Safety Items

- Safety glasses
- A mask
- A small fan

An open window, or a suitable outdoor/semi-outdoor space, i.e. a garage



Extra Credit!!

Bus pirate

Interfaces for many of your favorite serial communication protocols: JTAG, SPI, UART, I2C, etc.




- Provides a stable environment for running utilities like flashrom
- Also a good environment for reverse engineering ARM binaries without the need for an emulator like **QEMU**
 - Extra Extra credit if you run your Raspberry Pi with the Kali re4son kernel!



Confirm UART headers

Confirm TX, RX, GND and VCC pins Confirm voltage reading on pins matches specs Test with serial console



Drawing identified components and traces on the PCB



Drawing identified components and traces on the PCB



Connect to pins on Flash Chip

Confirm pinout of chip (CS, SO, WP, GND, VCC, RESET, CLK and SI pins)
 Solder wires to SO, SI, CLK, CS pins
 Attach wires to test clips on Bus Pirate





dump firmware from flash chip with flashrom

root@kali:~# flashrom -p buspirate-spi:dev=/dev/ttyUSB0,spispeed=115200 -r flash.bin

Trash / otw dc207CTF

est ing_resourc..._academy

References **References for this talk**

 "Major Vulnerabilities and Exploit Found in Foscam Cameras" Or Peles VDOO <u>cameras</u>

 "decrypt-foscam.py" bashis Github <u>https://github.com/mcw0/PoC/blob/master/decrypt-foscam.py</u>

<u>https://www.vdoo.com/blog/vdoo-has-found-major-vulnerabilities-in-foscam-</u>



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